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CL2 System Block Diagram (F Version, RAMP stage)

55-pin LCD Conn
(7.5" TFT)

Himax D-CON
HX8837-A-DS
18-bit LCD

Realtek I2S
Audio Codec
ALC5631
I2S

ENE EC
IO3731
(64p)

PS2 x2

SDI (as SPI)

TWSI3

SPI Flash (8Mb)

SD/MMC[2]

JTAG

USB_OTG

USB[3:1]

USB[4]

Mini-PCle Socket
(WLAN/WWAN)

Genesys Logic
USB Hub
GL850G

Touch Screen IC

TWSI4

SPI Flash (8Mb)

SD/MMC[3]

TWSI6

GPIO (as I2C)

Digital Compass IC

Marvell
ARMADA 610
88AP688

ARM v6/v7 CPU
640 Pin FCCBGA
21X21m package
06.5mm ball pitch

24-bit LCD
HDMI 1.3a x1
MIPI DSI x2
MIPI CSI-2 x2
I2S/AC97; SPDIF
32-bit (LP)DDR1/2
32-bit DDR3
Static Memory
16-bit NAND FLASH
4/8-bit SD/MMC x4
MIPI HIS x1
MIPI SLIMbus
USB 2.0 (HS) x2
USB 2.0 (ULPI) x1
USB 2.0 (OTG) x1
MS-Pro x1; SSPs x2
TWSI x6; UART x4

One-Wire; PWM x4
USIM x1; 8x8 Keypad
TPIU x1

20-pin Camera Conn
(Camera module)

20-pin Camera Conn

CCIC1

GPIO (as I2C)

DDR3

DDR3 Chip (2GB max)
4 or 8 128Mb/256Mb x8

DDR3

eMMC

eMMC Chip (4/8GB)
(2) 2/4Gb x8

SD/MMC[3]

13-pin Card Reader
Int. Slot1 (SD Card)

SD/MMC[1]

13-pin Card Reader
Ext. Slot2 (SD Card)

SD/MMC[2]

 UART[1]

OLPC, Quanta
Debug Conn (JTAG)

JTAG

UART[3]

 UART Debug Conn

TWSI6

ST Accelerometer IC
LIS33DETR

GPIO (as I2C)

Digital Compass IC

Quanta Computer Inc.

PROJECT : CL2

SYSTEM BLOCK DIAGRAM

Date: Monday, December 12, 2011
For Reference Only
Updated on 2010/8/10
Layout: Place resistor near processor

JTAG & UART Debug Port

UART Serial port - debug connector

Serial port - debug connector

Quanta Computer Inc.

ARMADA 610 (2/5) INTERFACES

Project: CL2

Date: Monday, December 12, 2011

Sheet 1 of 20
ARMADA 610 (3/5) DDR3 & NAND

Schematic Diagram

Locate these termination resistors next to their associated pins of DRAM chip.
Address/Control/Clock Terminations

- M_A[15]
- M_A[14]
- M_WE#
- M_RAS#
- M_CAS#
- M_ODT
- M_CKE0
- M_CKE1

Resistor termination R49 don't be populated, and add a resistor 443 pull down.

8 capacitors for each DRAM chip

DDR3 Power Decoupling

- +1.5V_DDR3
  - C84: 10uH/6.3V/X5R_4
  - C81: 0.1uH/10V/X5R_4
  - C80: 0.1uH/10V/X5R_4
  - C82: 0.1uH/10V/X5R_4
  - C86: 0.1uH/10V/X5R_4
  - C137: 0.1uH/10V/X5R_4
  - C72: 0.1uH/10V/X5R_4
  - C79: 0.1uH/10V/X5R_4
  - C79: 0.1uH/10V/X5R_4
  - C83: 0.1uH/10V/X5R_4
  - C88: 0.1uH/10V/X5R_4
  - C109: 0.1uH/10V/X5R_4
  - C108: 0.1uH/10V/X5R_4
  - C111: 0.1uH/10V/X5R_4
  - C115: 0.1uH/10V/X5R_4
  - C104: 0.1uH/10V/X5R_4
  - C154: 0.1uH/10V/X5R_4
  - C150: 0.1uH/10V/X5R_4
  - C155: 0.1uH/10V/X5R_4
  - C140: 0.1uH/10V/X5R_4
  - R112: 49.9/1%_4
  - R89: 49.9/1%_4
  - R83: 4.7k/1%_4

Quanta Computer Inc.

Date: Monday, December 12, 2011
Sheet: 11 of 20

Project: CL2

DDR3 TERMINATION
Ext. SD2 Card Reader

**SD2 EXTERNAL PULL UP**

**LAYOUT:**
Close to Connector with Short Stub

1: Power off
0: Power on

---

Int. SD1 Card Reader

**SD1 EXTERNAL PULL UP**

**LAYOUT:**
Close to Connector with Short Stub

1: Power off
0: Power on

---

**Quanta Computer Inc.**

**PROJECT:** CL2

**MICRO SD & SD SLOTS**
SOC CORE POWER (+VCORE)

<table>
<thead>
<tr>
<th>VID1</th>
<th>VID2</th>
<th>+VCORE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1.4V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1.33V</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>1V</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>1V</td>
</tr>
</tbody>
</table>

Depend on GPIO PIN

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PWR (3/6) +1.8V+VCORE
1118 Solve one second noise during boot.

Vout=(V1+R1/R2)

Close to Pin 4 of G91711U

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For Reference Only
Updated on 2010/8/10

Power on sequence

(1) +VIN
(2) +3.3VSUS
(3) PWR_BTN#
(4) EN_MAIN_PWR
(5) +5V, +3.3V, +10V_GATE
(6) EN+_1.8V
(7) (AVDD_18_PLLM) +1.8V
(8) EN_VCORE_PWR
(9) +VCORE
(10) EN+_1.8V_PMIC
(11) +1.8V_PMIC
(12) (Active High) EN_xxx_PWR
(13) (Active Low) EN_xxx_PWR#
(14) Remaining Powers
(15) ALL_PWRGD
(16) EXT 32K
(17) (SOC_RESET#) RESET_INn
(18) (SYS_RESET#) Int. Reset
(19) Logic State
(20) VCXO_EN
(21) VCXO_IN

Pink signals from EC
Blue signals from SOC
Black signals from others

T1 < 50us
T2 < 100us
T3 > 150us
T4 > 0us
T5 > 0us
TvCxoST < ~7ms
Schematic modify Item and History :

A1-->A2

1. Design issue -

Page 4
a. Change U4 from 1338-31 to 1338-18
b. Change the VCC_RTC from +1.8V_PMIC to +1.8V_GPIO
c. Delete some reserved resistor for 1338-31

Page 5
a. Add Game button function on GPIO of Soc.
b. Change the USB power control from Soc to EC.
c. Change R94 from 0 ohm to 22 ohm; R88 need to close to the CH7.
d. Modify the GFPDATA0-5 to GFPDatab=6.

Page 6
a. Add "Boot device selection".
b. Modify the footprint of U10.
c. Populate R87 and depopulate D6.
d. Change the GPIO_71/72 from EC_SCL/SDA to SOC_KBD_CLK/SDA.

Page 7
a. Add eMMC function on Soc.
b. Change the C90 form 0.1uf to 100pf

Page 8
a. Depop R46.
b. Change the AVDD_USB from +3.3V_USB_HUB to +3.3V_SOC
c. Change the VCC_IO_SDMMC from +3.3V_SD to +3.3V_SD2

Page 13
a. Change the p/n of Y1
b. Modify the GFPGDATA0=5 to GFPGDATA1=6.

Page 14
a. Change the Audio IC from ALC5624 to ALC5631Q.
b. Pop R36.

Page 15
a. Change the pulled up voltage of R39 from +1.8V_AUDIO to +3.3V_SOC
b. Change the R179/R173 from 220ohm 0204 to 470ohm 0805.
c. Modify the schematic of internal microphone.
d. Add CN24 for Tactile Feedback

Page 17
a. Change Micro-SD socket to ext. SD.

Page 18
a. Change the NAND flash to eMMC.

Page 20
a. Pulling up the SDDA_CMD with R250 for WLAN function.

Page 21
a. Change 3.3V_USB_HUB to +3.3V_USB_HUB on decoupling capacitors of IC.

Page 22
a. Change the camera power IC.
b. Short between U5.20 and U5.24 : Short t between U5.19 and U5.25.
c. Add touch screen connector. (CN22)

Page 23
a. Adding 4 game buttons.

2. ESD/EMI -

Page 24
a. Reserve the ETV2 on BT1
b. On page12, adding some capacitors for EMI's request.
Schematic modify Item and History:

A2-->A3

1. Design issue -
Page 4
a. Change R29 to 330 ohm, and C227 to 10 uF to fix #10999.

Page 5

2. Modify by supplier -
a. Change +3.3VAUDIO to +3.3VAVDD everywhere it appears to fix #10974.

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Schematic modify Item and History:

B --> C

1. HW Changes -

Page4
- Add Q16 2N7002W and change C227 from 10uf to 1uf, R29 from 330ohm to 47ohm to fix spec issue
- delete C224/C219 for time accuracy.

Page5
- Add MEM_GPIO0 and GPIO1 to verify memory size
- add pull-up resistors (R156/R158) on G_sensor I2C bus
- depopulate R159 for customer's request

Page6
- Add SELLP_IND for suspend/resume function
- Delete Mavrell's debug circuit.
- delete a reserved 32.768kHz circuit.

Page7
- Add CAM_PWRDN to control 2'nd source of camera

Page13
- Change L22/L23/L30/L28/L27 for EOD issue.
- Delete some 0 ohm.

Page15
- Delete 10uf C235/C215/C167, and change C232/C230 to 2.2uf to meet the latest schematic
- Change C307 to 1uf

Page16
- Add R387/R388 2k to meet the latest schematic
- delete Tactile Feedback circuit

Page17
- Modify the ext. SD (add a pin to connect shideing)
- Add RC delay circuit and Change C279/C310 from 10uf to 4.7uf to avoid inrush current
- Using push-push type (CN26) and hinge type(CN25) to replace orignal ext. SD.

Page18
- modify the bypass capacitores on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page19
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page20
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page21
- modify the size of C269

Page22
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page22
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

2. Power changes -

Page25
- fine tune some components' values.
- change PD31 for customers' request

Page26
- add a 22uf on +3.3V

Page27
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page28
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page29
- modify the bypass capacitores on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page30
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page31
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page32
- modify the size of C269

Page33
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page34
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page35
- fine tune some components' values.
- change PD31 for customers' request

Page36
- add a 22uf on +3.3V

Page37
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page38
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page39
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page40
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page41
- modify the size of C269

Page42
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page43
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page44
- fine tune some components' values.
- change PD31 for customers' request

Page45
- add a 22uf on +3.3V

Page46
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page47
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page48
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page49
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page50
- modify the size of C269

Page51
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page52
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page53
- fine tune some components' values.
- change PD31 for customers' request

Page54
- add a 22uf on +3.3V

Page55
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page56
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page57
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page58
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page59
- modify the size of C269

Page60
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page61
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page62
- fine tune some components' values.
- change PD31 for customers' request

Page63
- add a 22uf on +3.3V

Page64
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page65
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page66
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.

Page67
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page68
- modify the size of C269

Page69
- Change the U15 because EOD issue
- depopulate R217 for 2'nd source.

Page70
- add a RC delay circuit for inrush current
- Change the controlled OLS_LED circuit from WLAN_LED to storage LED

Page71
- fine tune some components' values.
- change PD31 for customers' request

Page72
- add a 22uf on +3.3V

Page73
- pull-up a resistor 10k on VID_1
- connect EN_+1.8V_GPIO to Q16.2

Page74
- add a 22uf on +3.3V_eMMC_VCC/ and +3.3V_eMMC_IO

Page75
- Modify the LV_SET, PWR_LMT_ON#, LED_INHIBIT# and OLS_CATHODE
- add a 2.2uf on EC_RST# to fix boot issue
- Change the EC_ID table
- add a suspend./resume circuit
- delete another OLS circuit.
Schematic modify Item and History:

C --> D

1. HW Changes -

   All Page
   1. Delete some 0 ohm.

   Page5
   1. Fine tune the damping resistor for the signal quality of ext.SD and int.SD.

   Page15
   1. Add a RC filter circuit, and close to Audio codec for speaker noise
   2. Fine tune the trace spacing of speak out

   Page16
   1. Change TVS on Headphone for ESD
   2. Add a 100pf on int. MIC and two ground shedding on ext. SD for EMI

   Page17
   1. Modify the position of reserved int. SD(CN25) for shorting issue between CN25 and CN26.

   Page23
   1. Using dual-LEDs to instead of signal-LED on OLS
   2. Populate R351~R354 for dropping key issue after resume.

2. Power changes -

   All Page
   1. Delete some 0 ohm.

   Page28
   1. Add a power control of DDR3 termination for reducing the power consumption during suspend.

   Page25
   1. Change ISL9519_GND to GND on ACOK of charge IC.