20091116 1.20 leave the overshoot of clock

Quanta Computer Inc.
PROJECT : CL1B

IC9UM701 ON : 0 GFF : 1

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

+3.3V

**SMBus ADDRESS : D3**

20100122
Test point must be on the same side.

Put the caps. on the bottom of CPU.
Please refer to the placement below.

CPU C7M POWER&GND

Quanta Computer Inc.

PROJECT : CL1B

CPU C7M POWER&GND

Date: Friday, October 08, 2010
Termination resistor

Layout Notes:
placement between

20091119 For 512MB, de-populate
USB power / port

Reset circuit
Very loud whining when connected to a solar panel.

20090602 delete

102910113 By do draw as additional current from battery.

2009/06/02 change the R_VA2

2003/06/02 change part number

20090602 modify

2009/06/02 change torque from 5% to 1%

2003/06/32 modify

20101007 add another voltage divider

Very loud whining when connected to a solar panel

Constant Voltage Mode
Input Limit 10V

Input Detec 9.16-9.3V

QUANTA CONFIDENTIAL
2009/08/03 Delete Jump

2009/07/15 Modify power sequence and add discharge circuit

2009/12/24 Add MAX1776 schematics, Co-lay with PU8(TPS62050)

PR92 --> 165K (CS41652FB06)

20100310 boot problems properly.

2009/06/04 modify AGND to GND

2009/11/26 Add USBVCC discharge

2009/12/24 Add MAX1776 schematics, Co-lay with PU8(TPS62050)

2009/12/24 Add MAX1776 schematics, Co-lay with PU8(TPS62050)

2009/07/19 Add USB_PWR_EN (15,25)

2009/08/03 Delete Jump

2009/07/15 Modify power sequence and add discharge circuit

2009/12/24 Add MAX1776 schematics, Co-lay with PU8(TPS62050)

2009/12/24 Add MAX1776 schematics, Co-lay with PU8(TPS62050)

2009/07/19 Add USB_PWR_EN (15,25)
Vo = 0.8 \times (1 + (R_2/R_3))
9/15 Modify

9/16 Modify

Pin 41 is GND Pin

Rpullup=V/2.6mA-rdson=(3.3-0.05*3.3)/3m-15=1.33K

Rdroop=2.3*Droop*Risen/Rdson

Vin=Iocset*1.75V/175K=10uA

Risen=(Iocset*Rdson*0.2175)/Iocset-2uA-130

Risen=(9*11m*0.2175)/(10uA-2uA)=130=2.56K

VID0-VID5 do not have internal pull-up or pull-down capability.

Quanta Computer Inc.
Schematic modify Item and History:

A1-->A2

1. **DCON POWER**
   - A. Change PQ9.B pin from DCON_1.8 to DCON_EN
   - B. Change PQ13.G pin from DCON_EN to PQ12.C
   - C. Change PQ17.G pin from VDDEN to LCD_AVDD

2. **SB strapping**
   - A. Change R27, R83, R270, R54, R34, R87, R78 and R82 from 4.7K ohm to 1K ohm.

3. **Design issue**
   - A. The D pin and S pin of Q8 and Q12 is inverse
   - B. Change C299 part number
   - C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37
   - D. Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
   - E. RTC issue: VIA recommend to delete R216

4. **Power**
   - A. **1.8VSUS**
     - a. Add off-page connector: VR_ON
     - b. Modify FU5 pinout.
     - C. For +1.8VSUS sense: stuff PR15; don't stuff PR27 and PR26
     - D. For +1.8VSUS OCP: modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
     - E. modify FU1 pin11 net name to VR_ON
   - B. **+VCORE**
     - a. For SYSOK FULL HIGH: Stuff PR45
     - b. For +VCORE sense: don't stuff PC3 & PR3; stuff PR51 & PR52
     - C. For CPU Load line: for meet load line –1mV/A, modify PR52 & PR50 from 1K to 680 ohm
   - C. **1.2 and +VCORE**
     - a. Modify power good circuit: change net name from 3.3VSUS to +3.3VSUS
   - D. **Charger**
     - a. Delete clamp circuit (PR118, PD18, PQ38, PR124): FU12 (MB39A129) can guaranty to 28V
     - b. connect FU12 pin21 to PQ36 pin1,2,3 directly
     - c. change PR126 to 100K
   - E. **RTC**
     - A. VIA recommend to delete R216
   - F. **WLAN**
     - Change WLAN solution from SD card to TM100 module. See page 24
Schematic modify Item and History:

A2-->B1

2. SDIO
   A. SDIO: Micro SD
   B. SDIO1: SD Card Reader
   C. SDIO2: WLAN module

2. SB straping -
   A. Change R58, R170 and R195 pull up power plane on page13

3. Design issue -
   A. Modify CPU RST circuit
      a. Add R248 0 ohm
      b. Populate Q18, Q20 R275 to prevent leakage for vendor's recommend.
      c. Del c299 for CPU power good delay time
   B. Del SPI ROM of memory
   C. Modify DCONLOAD and WLAN_RESET# to U19.AG20 and AF21
   D. Modify Serial enable to U19.AJ21
   E. Modify TBN# pin of U19 from PROCHOT# to ER_MODE
   F. Del EDID_CLK and EDD_DATA of CRT circuit
   G. Del R195 within GDATA0 pull low
   H. Reverse C436, C438, C233 and C232 for EMI/ESD
   I. Add PC120 and PC121 for VH gilch and add D36 to prevent 3VPU forward to +1.8VSUS
   J. Move C250 to close CON2 and modify CAM LED control.
   K. Del NAND flash on page 22
   L. Add PWRGD net on U28.17 & SYSOK on U28.4 & change M/B ID & Del SW7 on page 23
   M. change Q14 from NPN BJT to P-MOS
   N. Change WLAN solution from on board to slot and correct WLAN LED behavior on page 24.
   O. Add Micro SD on page 24.
   P. Correct power good circuit on page 25.

4. Power -
   A. Del all jump, but only reserve the jump of +VCCORE and +1.8VSUS.
   B. +1.8VSUS
      a. Add off-page connector : VR_ON
      b. Modify F05 pinout.
      c. For +1.8VSUS OCP : modify PR22 from 4.99K to 6.2K, OCP from 3A to 3.5A
   B. +VCCORE:
      a. For SYSOK FULL HIGH: Stuff PR45
      b. For +VCCORE sense: don't stuff PC3 & PR3; stuff PR51 & PR52
      c. For CPU Load line : for meet load line -1mV/A, modify PR52 & PR50 from 1K to 680 ohm
   D. Charger:
Schematic modify Item and History:

B2-->B3

1. **Power** -
   A. Change PL11 from 4.7uH to 15uH
   B. Delete PJP5

2. **Design issue** -
   A. Correct part reference from 12 to U24
   B. Change C299 part number
   C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37
   D. Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
   E. RTC issue: VIA recommend to delete R216

1. **DCON POWER** -
**Schematic modify Item and History:**

C1--->C2

1. **Power** -
   - A. PU6/PU7 (AOZ1021): correct the R/C of comp pin to 11K and 2.2nF
   - B. Change the PQ21 from CHDTC144U to ME1304AT3 (Vgs<1V)
   - C. Correct the +3.3VSUS to 3VPCU on PR69.1 and PR62 for prevent the +1.2V_GD glitch
   - D. Change the Q13 and PQ31 to AO3404 for power good glitch by +3.3V & 5V sequence issue on PU3
   - E. Add MAX1776 circuit for TPS62050 L/T time isn't enough.
   - F. Correct the +1.2V discharge circuit

2. **Design issue** -
   - A. Correct part reference from 12 to U24
   - B. Change C299 part number
   - C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37
   - D. Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
   - E. RTC issue: VIA recommend to delete R216

   **Schematic modify Item and History:**

   1. **Power** -
      - A. Reserve PC123, PR164.
      - B. Short the PU8.2 & PU8.6 to GND for Vin_OK keep high

   2. **Design issue** -
      - A. Correct part reference from 12 to U24
      - B. Change C299 part number
      - C. Add test points: U28, pins 1, 4, 17, 29, 36, and 37
      - D. Change U29 pin 37,36 net name from MIC1_R & MIC_L to MIC2_R & MIC2_L
      - E. RTC issue: VIA recommend to delete R216
1. **Boot problems:**
   
   PR31 : 22ohm -> 10ohm. (10 ohm is normal value.)

2. **Flash problems:**
   
   Add pull-up resistor R396 (4.7k 0402).

3. **Very loud whining when connected to a solar panel**
   
   Replace PD22 to schottky diode and invert it (the cathode of PD22 connect to PR152/PC102).
   
   PC102 - 0.47uF, 6V, 0402, Y7V
   
   PR116 - 475K, 1%, 0402
   
   PR117 - 28K, 1%, 0402
   
   PR120 - 28K, 1%, 0402
   
   PR125 - 2.2K, 5%, 0402
   
   PR126 - 2.2K, 5%, 0402
   
   PR144 - 330K, 1%, 0402