<table>
<thead>
<tr>
<th>PAGE</th>
<th>DESCRIPTION</th>
<th>PAGE</th>
<th>DESCRIPTION</th>
<th>PAGE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TITLE PAGE</td>
<td>19</td>
<td>Int. SD SLOTS1 &amp; Ext. SD SLOTS2</td>
<td>37</td>
<td>Schematic modify history B1</td>
</tr>
<tr>
<td>2</td>
<td>SYSTEM BLOCK DIAGRAM</td>
<td>20</td>
<td>eMMC FLASH (MLC)</td>
<td>38</td>
<td>Schematic modify history C</td>
</tr>
<tr>
<td>3</td>
<td>POWER SEQUENCE</td>
<td>21</td>
<td>EC IO3731</td>
<td>39</td>
<td>Schematic modify history D</td>
</tr>
<tr>
<td>4</td>
<td>RTC BATTERY &amp; RTC CLOCK</td>
<td>22</td>
<td>WLAN MODULE (SDIO)</td>
<td>40</td>
<td>Power Rail</td>
</tr>
<tr>
<td>5</td>
<td>MMP3 (1/7) GPIO</td>
<td>23</td>
<td>USB HUB &amp; PORTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>MMP3 (2/7) INTERFACES</td>
<td>24</td>
<td>CAMERA &amp; G-SENSOR &amp; TOUCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>MMP3 (3/7) DDR3_0 &amp; NAND</td>
<td>25</td>
<td>TPD/KBD/LED/SENSOR/BUTTON</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>MMP3 (4/7) DDR3_1</td>
<td>26</td>
<td>NEONODE TOUCH</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MMP3 (5/7) PWR</td>
<td>27</td>
<td>HDMI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MMP3 (6,7/7) VSS &amp; VCORE</td>
<td>28</td>
<td>POWER MAP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DDR3_0 SDRAM</td>
<td>29</td>
<td>PWR (1/6) CHARGER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>DDR3_1 SDRAM</td>
<td>30</td>
<td>PWR (2/6) +3.3VSUS/+5V/+3.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>DDR3 TERMINATIONS</td>
<td>31</td>
<td>PWR (3/6) +1.8V/+VCORE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>RESET CIRCUIT/HOLES</td>
<td>32</td>
<td>PWR (4/6) DDR3 PWR/+1.2V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>DCON HX8837</td>
<td>33</td>
<td>PWR (5/6) LED BACKLIGHT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>LCD CONNECTOR</td>
<td>34</td>
<td>PWR (6/6) DISCHARGE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>I2S AUDIO CODEC ALC5631Q</td>
<td>35</td>
<td>POWER SEQUENCE TIMING</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>AUDIO JACKS</td>
<td>36</td>
<td>Schematic modify history A2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Marvell
MMP3 2128

ARM v6/v7 CPU
783 Pin HFCBGA
19X19m package
0.65mm ball pitch

24-bit LCD
HDMI 1.3c+3D x1
MIPI DSI x2
MIPI CSI-2 x2
I2S/AC97; SPDIF
32-bit (LP)DDR1/2
2X32-bit DDR3 Dual
Static Memory
16-bit NAND FLASH
4/8-bit SD/MMC x5
MIPI HIS x1
MIPI SLIMbus
USB 2.0 (HS) x2
USB 2.0
(ULP/FSIC/OTGI) x1
USB 3.0 X1
WDT,RTC 2times
SSPs x4; SPIx4
TWSI x6; UART x4
10/100 FE with FHY
One-Wire; PWM x4
USIM x1; 8x8 Keypad
TPIU x1
For Reference Only

Updated on 2012/07/12

Pink signals from EC
Blue signals from SOC
Black signals from others
Quanta Computer Inc.

PROJECT : CL2

ARMADA 610 (3/5) DDR3 & NAND

Layout: Place as close as possible to SoC
2Gb BOT Side

2Gb TOP Side

Quanta Computer Inc.

DDDR3 96ball x16 list...
HYU - 2Gb x16 – AKDSMGTW04 – V
CH0 Address/Control/Clock Terminations

CH1 Address/Control/Clock Terminations

DDR3 Power Decoupling

Follow Marvell's schematic

NOTE: Place caps next to package and near pall

Resistor termination 869 don't be populated, and add a resistor R83 pull down.
Ext. SD2 Card Reader

SD Write Protect Detection
(0: Write Enable; 1: Write Protect)

Int. SD1 Card Reader

PUSH-PUSH TYPE

Hinge Type

SD Write Protect Detection
(0: Write Enable; 1: Write Protect)
On HUB 7, 7.3.2 is generated by V5 if using internal LDO.
**Power on sequence**

**OFF**

**For Reference Only**

Updated on 2012/7/11

1. **+VIN**
   - **Ta**
   - **Tb**
   - **Tc**
   - **Td**

2. **+3.3VSUS**
   - **PWR_BTN#**
   - **EN_MAIN_PWR**

3. **+5V, +3.3V, +10V_GATE**
   - **EN_VCORE_PWR**

4. **+VCore**
   - **(Analog_PWR)**
   - **+1.8V**

5. **EN+_3.3V_SOC#**
   - **+3.3V_SOC**

6. **EN+_1.8V_PMIC#**
   - **+1.8V_PMIC**

7. **EN+_1.8V_GPIO#**
   - **+1.8V_GPIO**

8. **EN_NAND_SOCGPIO#**
   - **+3.3V_NAND**

9. **EN+_3.3V_SD2**
   - **+3.3V_SD2**

10. **EN+_1.2V_SOC**
    - **+1.2V_SOC**

11. **EN+_1.5V_DDR3**
    - **+1.5V_DDR3**

12. **ALL_PWRGD**
    - **VCXO_EN**

13. **(SOC_RESET#) RESET_INn**
    - **PRI_TRST**

14. **(SYS_RESET#) Int. Reset**

**Pink signals from EC**

**Blue signals from SOC**

**Black signals from others**

- **T1** > 0ms
- **T2** > 0ms
- **T3** > 100us
- **T4** > 77us
- **T5** > 385us
- **T6** > 2ms
- **T7** ~ 2ms

**Project:** CL4

**Quanta Computer Inc.**
Schematic modify Item and History:

A2-->B1

1. Fixing +3.3V_SOC -
   1. Change PR79 to a 10K resistor

2. Fixing +3.3V_SOC -
   1. PR62 (or PR57) should be 12.0K
   2. PR67 should be 18.0K
   3. PR66 should be 120K
   4. PR73 should be 30.0K

3. Pulse JTAG Reset at start of day -
   1. Add a small schottky between EN_+1.35V_DDR3 and PRI_TRST#. The cathode of the diode should be connected to EN_+1.35V_DDR3.
   2. Remove the 100K resistor from R335.
   3. Populate R334 with a 100K resistor

4. Fix MMP3 B0 errata 1.15 -
   1. Replace R45 with a 10 ohm resistor (pref. 0603 or 0805)

5. Changing to a +1.8V SPI Flash -
   1...

6. Changing to a +1.8V SPI Flash -
   1. Remove the resistors from the following locations: R94 (3K), R98 (3K), R253 (3K), R258 (3K), R372 (1.2K), R373 (1.2K), and R375 (1.2K)
   2. Replace D18 with a 3K resistor
   3. Remove Q36, and place a 3K resistor between pins 1 and 3
   4. Remove Q38, and place a 3K resistor between pins 1 and 4
   5. Add a 3K pullup resistor to +3.3VSUS_EC (or +3.3VSUS) to EC_SDI_MISO (Q37, pin 3).
   6. Add a 3.6K pulldown from SDI_MOSI (D18 anode) to GND
   7. Add a 3.6K pulldown from SDI_CLK (Q36.1) to GND
   8. Add a 3.6K pulldown from SDI_CS# (Q38.1) to GND
Schematic modify Item and History:

B1 --> C1

1. Change footprint -
   1. Change C351, C354 and C355 from 0603 to 0402
   2. Change PC59, PC50, PC94, PC105, PC96, PC95, PC39 and PC38 from 0805 to 0603

2. EMI issue -
   1. Reserve a common choke L54 on USB_HUB_P/N
   2. Change common choke source on both USB ports.
   3. Add two bead (EMI FILTER MHC2012S8000BP (80, 5A)) between battery connector (CN22) and P-MOS (PQ58).
   3. Add C494 (330pf) to fix signal noise. Need to close R300
   4. Reserve a discharge circuit on eMMC power and a pulled-up resistor R101 on eMMC_RST to fix SDHCI error.

5. Add C487 (330pf) and C488 (330pf) to fix ESD air discharge issue

6. Using +1.8V SPI Flash -
   1. Populate U27 and remove Q36
   2. Add R413 (39 ohm) between SOC_SPI_CLK and SPI_CLK
   3. Change R295 to 1 kohm

7. Add C485 (0.1uf) to close U7.3 for fixing power noise.

8. Change the following resistors from 0 ohm to short -
   R118, R105, R101, R79, R237, R229, R263, R103, R36, R60, R303, R174, R175, R363

9. Remove TP76 and TP74

10. Pull-up R103 to +1.8V_SOC_PMIC on CLK_REQ for Marvell's suggestion.

11. Electrical/Environmental Test Specification -
    Add two serial resistors R409 (220hm) between L22 and HP_OUT-L, R410 (220hm) between L21 and HP_OUT-R.

12. Change R14.1 from +3.3V to +3.3V_NAND for sequence.

13. Using dual ext. SD power switch to support USH-I mode.

14. Reserve a cap C493 for CMD hold-timing

15. Modify MB_ID. Change R340 to 20k ohm.

16. Add a parallel cap C486 (47pf) on R400 to fix SOC/EC communications issue.

17. Error key issue -
   1. Change R386 and R392 from 0 ohm to ferrite bead (L53 and L52 with 220ohm).
   2. Reserve C489, C490, C491 and C492 on +VIN.

18. Inverse the CN5.

19. Add a decoupling cap C500 (0.1uf) on HDMIC_5V and close to CN14.19

20. Fix +VIN noise
    1. Add PC156 (10uf) on +VIN_5V_PAD.
    2. Add PC157 (10uf) on +VIN_3V_PAD.
    3. Add PC155 and PC75 (10uf) on +VIN_1.8V_PAD.

21. Change the control pin of ext. SD power discharge.
Schematic modify Item and History:
Schematic modify Item and History:
<table>
<thead>
<tr>
<th>Power Plane</th>
<th>Voltage</th>
<th>Description</th>
<th>Control Signal</th>
<th>S0</th>
<th>S3</th>
<th>S5</th>
</tr>
</thead>
<tbody>
<tr>
<td>+VADP_IN</td>
<td>+10.5V~+25V</td>
<td>Adapter In</td>
<td></td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>+3.3VBAT</td>
<td>+3.0V~+3.3V</td>
<td>RTC</td>
<td></td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>+3.3VSUS</td>
<td>+3.3V</td>
<td>EC POWER</td>
<td>+VIN</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>+5V</td>
<td>+5V</td>
<td></td>
<td>EN_MAIN_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V</td>
<td>+3.3V</td>
<td>RTC</td>
<td>EN_MAIN_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+10V_GATE</td>
<td>-9V</td>
<td>+3.3V power rail gate power</td>
<td>EN_MAIN_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_SOC</td>
<td>+3.3V</td>
<td>IO power of SoC</td>
<td>EN+3.3V_SOC#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_USBIN</td>
<td>+3.3V</td>
<td>IO power of SoC</td>
<td>EN+3.3V_NAND#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_SD2</td>
<td>+3.3V</td>
<td>IO power of SoC / ext. SD</td>
<td>EN_SD2_PWR#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_NAND</td>
<td>+3.3V</td>
<td>IO power of SoC</td>
<td>EN+3.3V_NAND#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_BB</td>
<td>+3.3V</td>
<td>IO power of SoC</td>
<td>EN+3.3V_NAND#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_USB_HUB</td>
<td>+3.3V</td>
<td>USB HUB</td>
<td>EN_USB_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+1.8V_PMIC</td>
<td>+1.8V</td>
<td>IO power of SoC</td>
<td>EN+1.8V_PMIC#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+1.8V_GPIO</td>
<td>+1.8V</td>
<td>IO power of SoC</td>
<td>EN+1.8V_GPIO#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+1.8V</td>
<td>+1.8V</td>
<td>IO power of SoC</td>
<td>EN_MAIN_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+5V_USB</td>
<td>+1.8V</td>
<td>IO power of SoC / USB_POWER</td>
<td>EN+5V_USB#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+1.2V</td>
<td>+1.2V</td>
<td>IO power of SoC</td>
<td>EN+1.2V</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+1.5V_DDR3</td>
<td>+1.5V</td>
<td>Memory power</td>
<td>EN+1.5V_DDR3</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+0.75VREF_DDR3</td>
<td>+0.75V</td>
<td>Memory power</td>
<td>EN+0.75V_DDR3</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+9.6V_LCD</td>
<td>9.6V</td>
<td>Analog power for LCD</td>
<td>EN_LCD_PWR</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+18V_GH</td>
<td>+18V</td>
<td>TFT on power for LCD</td>
<td>EN+18V_GH</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>-7V_GL</td>
<td>-7V</td>
<td>TFT off power for LCD</td>
<td>EN_LCD_PWR</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+1.8V_DCON</td>
<td>+1.8V</td>
<td>DCON</td>
<td>EN_DCON_PWR#</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+2.5V_DCON</td>
<td>+2.5V</td>
<td>DCON</td>
<td>EN+2.5V_DCON</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+VCORE</td>
<td>+1.33~+1.40V</td>
<td>SoC</td>
<td>EN_VCORE_PWR</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_WLAN</td>
<td>+3.3V</td>
<td>WLAN</td>
<td>EN_WLAN_PWR</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+1.8V_WLAN</td>
<td>+1.8V</td>
<td>WLAN</td>
<td>+3.3V_WLAN</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>+3.3V_SD1</td>
<td>+3.3V</td>
<td>eMMC</td>
<td>EN_SD1_PWR#</td>
<td>V</td>
<td>V</td>
<td>X</td>
</tr>
</tbody>
</table>