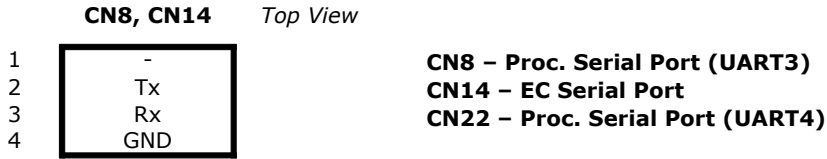


**Serial Interfaces**



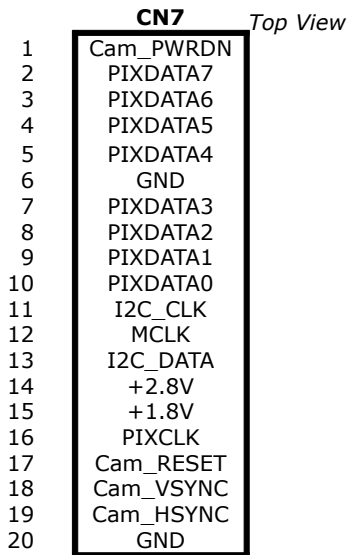
**SPI Interfaces**

**J2 – OFW SPI Flash Prog. Port !! +1.8V !!**  
**J3 – EC SPI Flash Prog. Port**

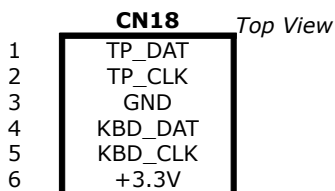


This pinout is used by J2 and J3 in the laptop. These are slave connectors, allowing in-system programming (ISP) of the onboard SPI Flash ROMs. This pinout is defined by Atmel App. Note AVR910.  
*Note: MOSI and MISO are swapped on J2 on the A2 prototypes*

**Camera**



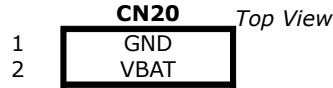
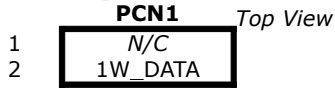
**Keyboard/Touchpad**



The keyboard and touchpad use PS/2 protocol interfaces

## Connectors

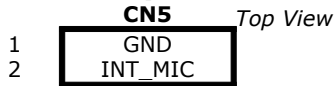
### Main Battery



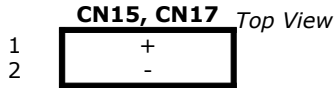
### RTC Battery



### Internal Microphone

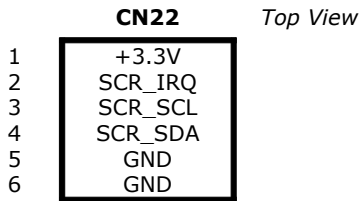


### Speakers

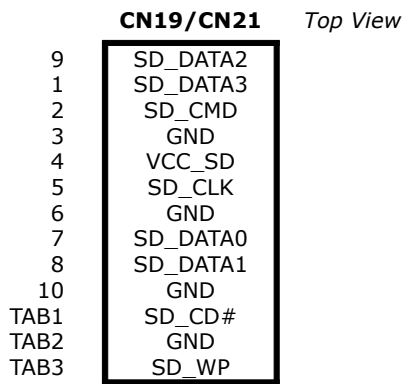


*Also used for CN24*

### Touchscreen

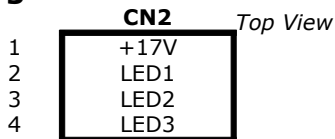


### Internal/External SD/MMC



The SD connector pins are not numbered sequentially. In addition, two of the signal pins (TAB1/TAB3) appear to be mounting tabs along the edge.

### Backlight



**Connectors**

**LCD**

CN1		Top View	CN1 (cont.)	
1	VCOM		29	GMA8-1
2	VCOM		30	GMA6-1
3	-7V		31	GMA5-1
4	+9.6V		32	GMA3-1
5	GND		33	GMA1-1
6	GMA10-2		34	GND
7	GMA8-2		35	+1.8V
8	GMA6-2		36	FD00
9	GMA5-2		37	FD01
10	GMA3-2		38	FD10
11	GMA1-2		39	FCLK
12	GND		40	FREV
13	+1.8V		41	FD11
14	BD00		42	FD20
15	BD01		43	FD21
16	BD10		44	FSTH
17	BCLK		45	FTP1
18	BREV		46	FPOL
19	BD11		47	VCOM
20	BD20		48	XAO
21	BD21		49	OE
22	BSTH		50	CKV
23	BTP1		51	STV
24	BPOL		52	+1.8V
25	VCOM		53	-7V
26	+9.6V		54	+18V
27	GND		55	GND
28	GMA10-1			

**WLAN Card**

CN10			Top View
1	GPIO4	+3.3V	2
3	BT_PRIORITY	GND	4
5	WL_ACTIVE	+1.8V	6
7	BT_STATE	TRST#	8
9	GND	TMS_CPU	10
11	-	TCK	12
13	-	TDO	14
15	GND	TDI	16
		<i>key</i>	
17	SD_CD	GND	18
19	GND	PD#	20
21	SD_CLK	RESET#	22
23	GND	+1.8V	24
25	SD_CMD	GND	26
27	SD_DAT0	+1.8V	28
29	SD_DAT1	-	30
31	SD_DAT2	-	32
33	SD_DAT3	GND	34
35	GND	USB-	36
37	GND	USB+	38
39	+3.3V	GND	40
41	SD_VCC	-	42
43	GND	LED_WLAN#	44
45	GPIO2	-	46
47	ECS#	SLEEP_CLK	48
49	TR3#	GND	50
51	ANT_SEL_N	+3.3V	52

*USB supplied but not used*

*SD\_VCC is +1.8V on XO-1.75*

### OLPC Debug (JTAG) Port

**CN6** *Top View*

1	+3.3V
2	+1.8V
3	JTAG_SEL
4	SOC_RESET#
5	SOC_TRST#
6	SOC_TMS
7	SOC_TCK
8	SOC_TDI
9	SOC_TDO
10	GND

### Marvell Debug (JTAG) Port

**CN13** *Top View*

1	GND	
2	GND	
3	GND	
4	+1.8V_SOC	
5	+1.8V_SOC	
6	+3.3V_SOC	
7	+3.3V_SOC	
8	JTAG_SEL	+1.8V
9	SYS_RESET#	+1.8V
10	SOC_RESET#	+1.8V
11	UART1_TXD	!!! +1.8V levels !!!
12	UART1_RXD	!!! +1.8V levels !!!
13	GND	
14	SOC_TRST#	+1.8V
15	SOC_TMS	+1.8V
16	SOC_TCK	+1.8V
17	SOC_TDI	+1.8V
18	SOC_TDO	+1.8V
19	GND	
20	GND	